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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,337	10/17/2003	Yan Borodovsky	10559/880001/P17482/Intel	2304
20985	7590	11/30/2006		
FISH & RICHARDSON, PC P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			EXAMINER CHACKO DAVIS, DABORAH	
			ART UNIT	PAPER NUMBER
			1756	

DATE MAILED: 11/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/688,337

Applicant(s)

BORODOVSKY, YAN

Examiner

Daborah Chacko-Davis

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 September 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) 9-15 and 30-36 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 16-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>01.03.05, 07.10/05; 02.07/06</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, claims 1-8, and 16-29, in the reply filed on September 1, 2006, is acknowledged. Claims 9-15, and 30-36, are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 7, 16-20, are rejected under 35 U.S.C. 102(b) as being anticipated by U. S. Patent No. 4,517,280 (Okamoto et al., hereinafter referred to as Okamoto).

Okamoto, in col 3, lines 12-54, discloses a method of patterning a substrate by forming a photoresist layer on the substrate, performing a first exposure by holographic exposure (interference lithography) to form an array of repeating line and space patterns (grating pattern), performing a second exposure via a mask (see figure 3(3)), thereby introducing irregularity (imparting the mask pattern or arbitrary arrangement) into the already formed repeating line and space patterns, i.e., reducing or ending the continuity of the array of the line and space pattern (grating pattern or trench pattern) (claims 1, 4, 16-17). Okamoto, in col 3, lines 25-55, and in figure 3, discloses forming

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an arbitrary figure (see reference B in figure 3(4), a second photoresist mask) above or in some portion of the array of line and space patterns (grating), and etching (patterning) the substrate through portions not covered by the second photoresist mask B (arbitrary figure) using the arbitrary arrangement (directs the etching or selective etching) i.e., reducing the continuity of the array of patterns by cutting spaces in the array and imparting or transferring the photomask or resist mask pattern onto the substrate (claims 2-3, 5, 7, 18-20).

4. Claims 1-2, 6, are rejected under 35 U.S.C. 102(b) as being anticipated by U. S. Patent No. 6,337,175 (Yamaguchi).

Yamaguchi, in col 5, lines 24-67, in col 6, lines 1-24, and in figures 2, 3, and 4, discloses a method of patterning a substrate by forming a photoresist layer on the substrate, performing a projection lithographic exposure (using a stepper) on the photoresist layer to form an array of line-and-space patterns, performing a second exposure by forming an arbitrary figure (using a second photomask, reference 5) above the array, thereby introducing an irregularity in the array of the line-and-space patterns and reducing the continuity of the portion of the array (see figure 4, the continuity of the array is reduced as a result of the second exposure using a mask different from that of the first exposure) (claims 1-2, and 6)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 8, and 21, are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Patent No. 4,517,280 (Okamoto et al., hereinafter referred to as Okamoto) in view of EP 0915384 (Sugita et al., hereinafter referred to as Sugita).

Okamoto is discussed in paragraph no. 3.

The difference between the claims and Okamoto is that Okamoto does not disclose the patterning of the substrate with the arbitrary arrangement uses a pitch yielding a k_1 factor smaller than 0.4 (claim 8). Okamoto does not disclose that the first interference exposure process uses a pitch that yields a k_1 factor approaching 0.25 (claim 21).

Sugita, in col 4, lines 1-41, discloses using a k_1 factor of less than 0.4 and that a k_1 factor as low as 0.25 can be used in an interference exposure process.

Therefore, it would be obvious to a skilled artisan to modify Okamoto by employing the pitch that generates the claimed k_1 factor as suggested by Sugita because Sugita, in col 3, lines 33-56, and in col 4, lines 1-15, discloses that the using the claimed k_1 factor i.e., less than 0.5 in an exposure process enables a higher resolution in the pattern and produces a fine periodic pattern that corresponds to the intensity distribution of the impinged light on the wafer.

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7. Claims 22-29, are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Patent No. 4,517,280 (Okamoto et al., hereinafter referred to as Okamoto) in view of EP 0915384 (Sugita et al., hereinafter referred to as Sugita).

Okamoto, in col 3, lines 12-54, discloses a method of patterning a substrate by forming a photoresist layer on the substrate, performing a first exposure (first lithographic technique) by holographic exposure (interference lithography) to form an array of repeating line and space patterns (grating pattern) having a first pitch, performing a second exposure via a mask (see figure 3(3), a second lithographic technique), thereby introducing irregularity or imparting a second pattern with a second pitch into the already formed repeating line and space patterns, i.e., reducing or ending the continuity of the array of the line and space pattern (grating pattern, eliminating the impact of some of the line and space pattern portions on the substrate) and wherein the second pitch is more than twice that of the first pitch (see figure 3) (claims 22-24, and 26). Okamoto, in col 3, lines 34-40, and in figure 3 (3), discloses performing a second exposure on the line and space pattern using a binary mask (a mask with part of the mask providing a light shielding section and the remaining part of the mask is a transparent section) so as to eliminate the impact (continuity) of the array of patterns (claim 25). Okamoto, in col 3, lines 25-55, and in figure 3, discloses forming an arbitrary figure (see reference B in figure 3(4), a second photoresist mask) above or in some portion of the array of line and space patterns (grating), and etching (patterning) the substrate through portions not covered by the second photoresist mask B (arbitrary figure) using the arbitrary arrangement (directs the etching or selective etching) i.e.,

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ending the continuity of the array of the line and space patterns or eliminating the impact of some portions of the line and space patterns by etching the exposed areas (not covered by the arbitrary figure viz., mask)(claims 27-29).

The difference between the claims and Okamoto is that Okamoto does not disclose that the first exposure process uses a pitch that yields a k_1 factor smaller than or equal to 0.5. Okamoto does not disclose that the first pitch yields a first k_1 factor approaching 0.25. Okamoto does not disclose that the second pitch yields a second k_1 factor greater than 0.5.

Sugita, in col 4, lines 1-15, discloses using a k_1 factor of less than 0.5 in an interference exposure process. Okamoto, in col 4, lines 16-20, discloses that a lithographic process can be performed using a k_1 factor greater than 0.5.

Therefore, it would be obvious to a skilled artisan to modify Okamoto by employing the pitch that generates the claimed k_1 factor as suggested by Sugita because Sugita, in col 3, lines 33-56, and in col 4, lines 1-15, discloses that the using the claimed k_1 factor i.e., at least less than 1.0 in an exposure process enables a higher resolution in the pattern and produces a fine periodic pattern that corresponds to the intensity distribution of the impinged light on the wafer.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daborah Chacko-Davis whose telephone number is (571) 272-1380. The examiner can normally be reached on M-F 9:30 - 6:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's

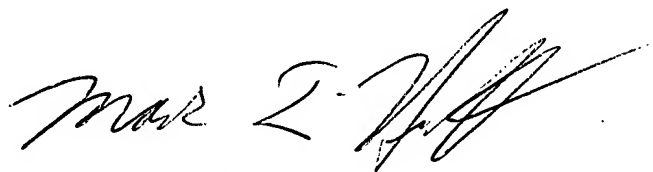
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supervisor, Mark F Huff can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

dcd

November 16, 2006.

A handwritten signature in black ink, appearing to read "Mark F. Huff", with a stylized flourish at the end.

**MARK F. HUFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700**